Modeling and Formal Verification of a Passive Optical Network on Chip Behavior

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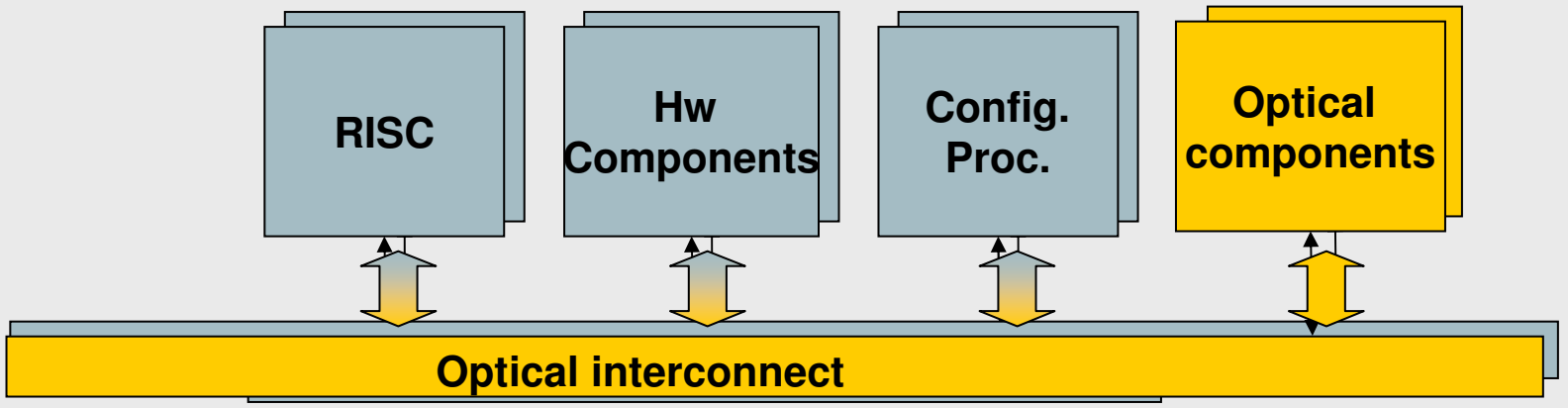
MPSoC interconnects



- *MPSoC interconnects challenges:*
  - Metallic interconnects will become the SoC bottleneck
    - Physical limits: propagation time (latency), power consumption
    - Amount of data to transfer between IP blocks
    - Heterogeneity (data flow, physical integration)

Optical Networks on Chip - An alternative

- High throughput in waveguide (~ THz)
  - Telecom techniques : wavelength routing
- Bidirectional waveguide
  - Network without contention
  - Routing congestion problems alleviated
- Crosstalk, capacitive loading and signal distortion are reduced
- Problem: heterogeneous integration of passive and active optical devices and IC for the conversion

Multi-domain design challenges

- Access to physical prototyping for multi-technology SoCs is a major challenge
  - Significant cost
  - Hard to influence standard processes
- Research is technology-dominated
  - Physical level research
  - New devices and architectures are defined
- High-level modeling and validation mandatory.
  - Few existing approaches
  - More research needed
- Cooperation between system-level and physical-level designers is required

Optical Networks on Chip

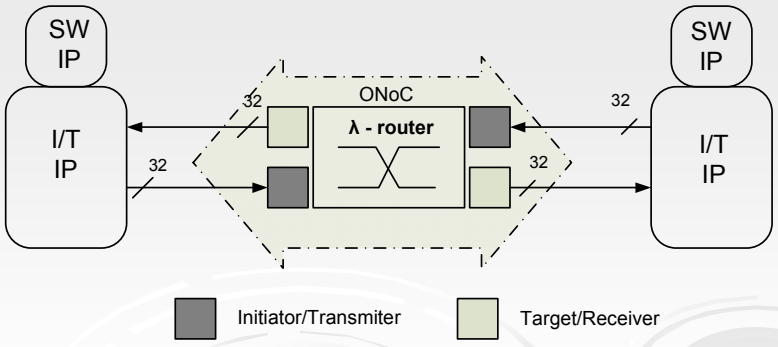
- *Contribution*:
  - A two step methodology for the modeling and the formal verification for the global validation of the behavior of a passive integrated photonic routing structure using models that are based on timed automata

Outline

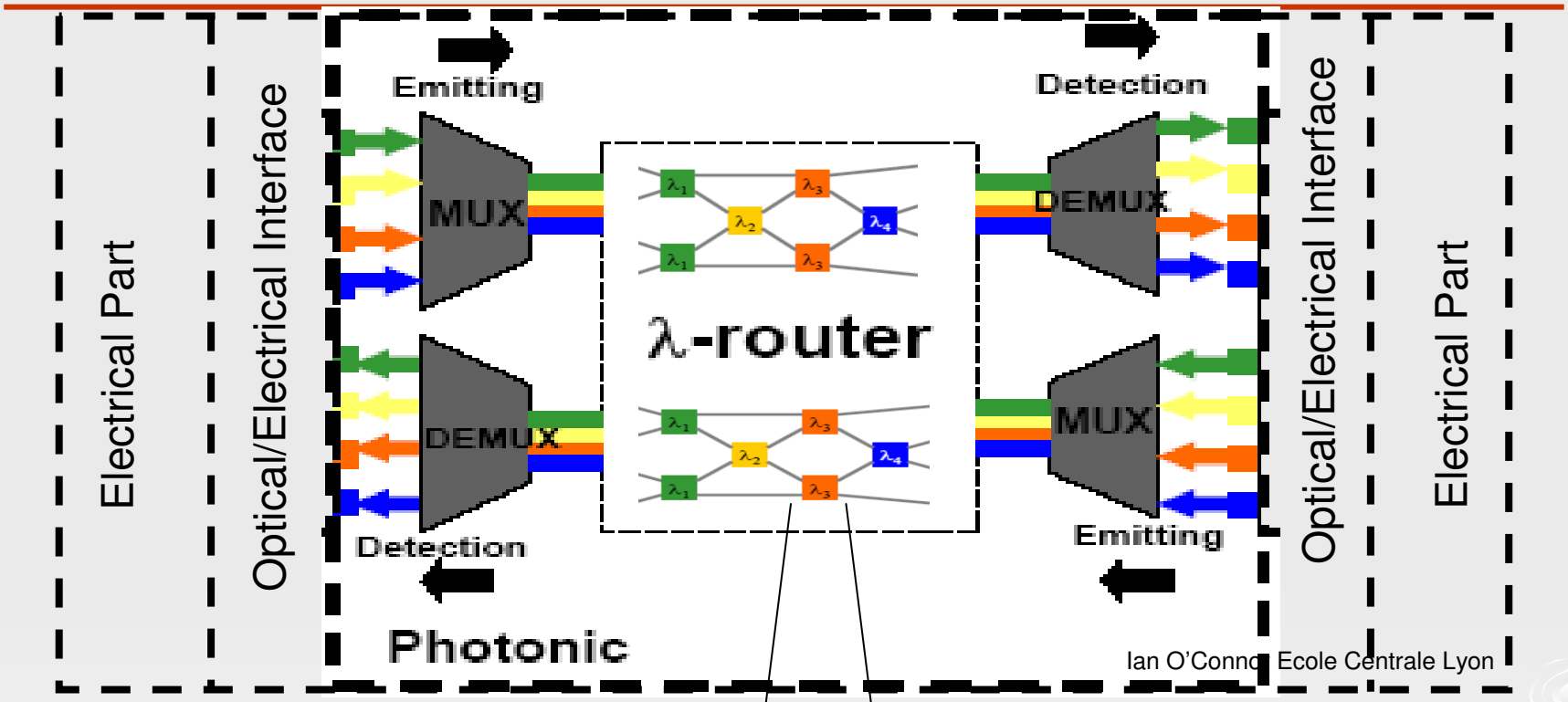
- **Basic concepts**
- Optical NoCs modeling and simulation
- Optical NoCs formal verification
- Conclusions

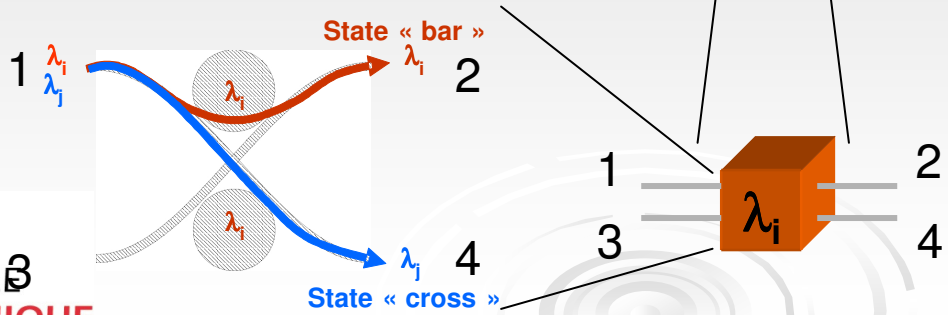
Optical Networks on Chip

- Each IP block (initiator and target) must send and receive data
  - Electro-optical conversion (EOC)
  - Opto-electrical conversion (OEC)
- Passive transport part: λ-router
  - Shared by all IP blocks to route the data through the network

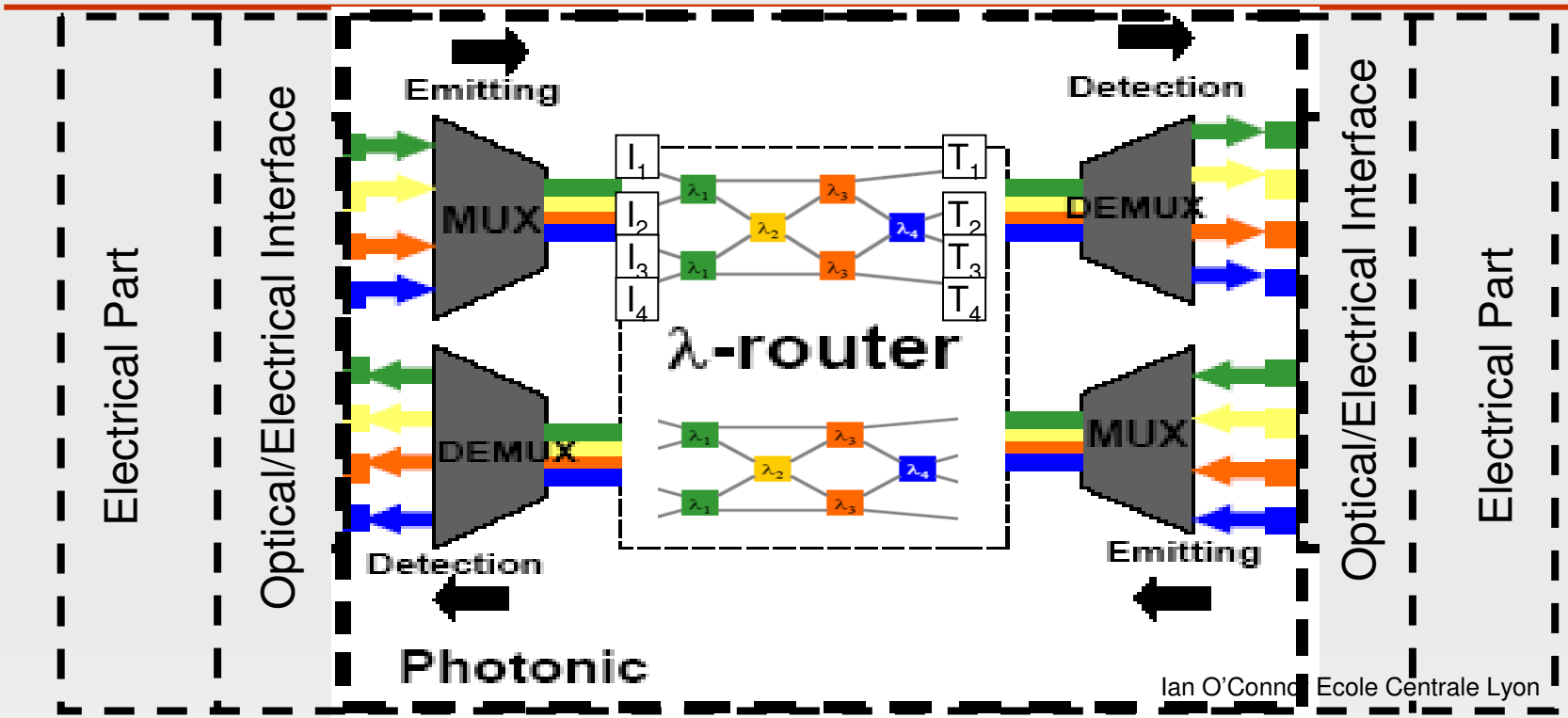


Optical NoC architecture

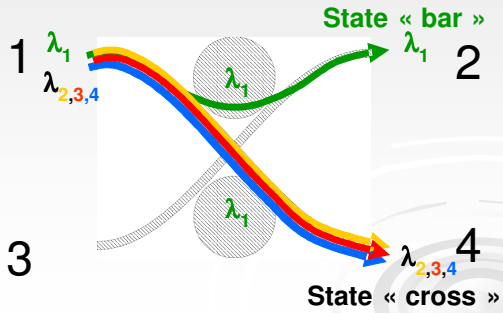




Optical NoC architecture



Ian O'Connor, Ecole Centrale Lyon



I/T	T_1	T_2	T_3	T_4
I_1	λ_2	λ_3	λ_1	λ_4
I_2	λ_3	λ_4	λ_2	λ_1
I_3	λ_1	λ_2	λ_4	λ_3
I_4	λ_4	λ_1	λ_3	λ_2

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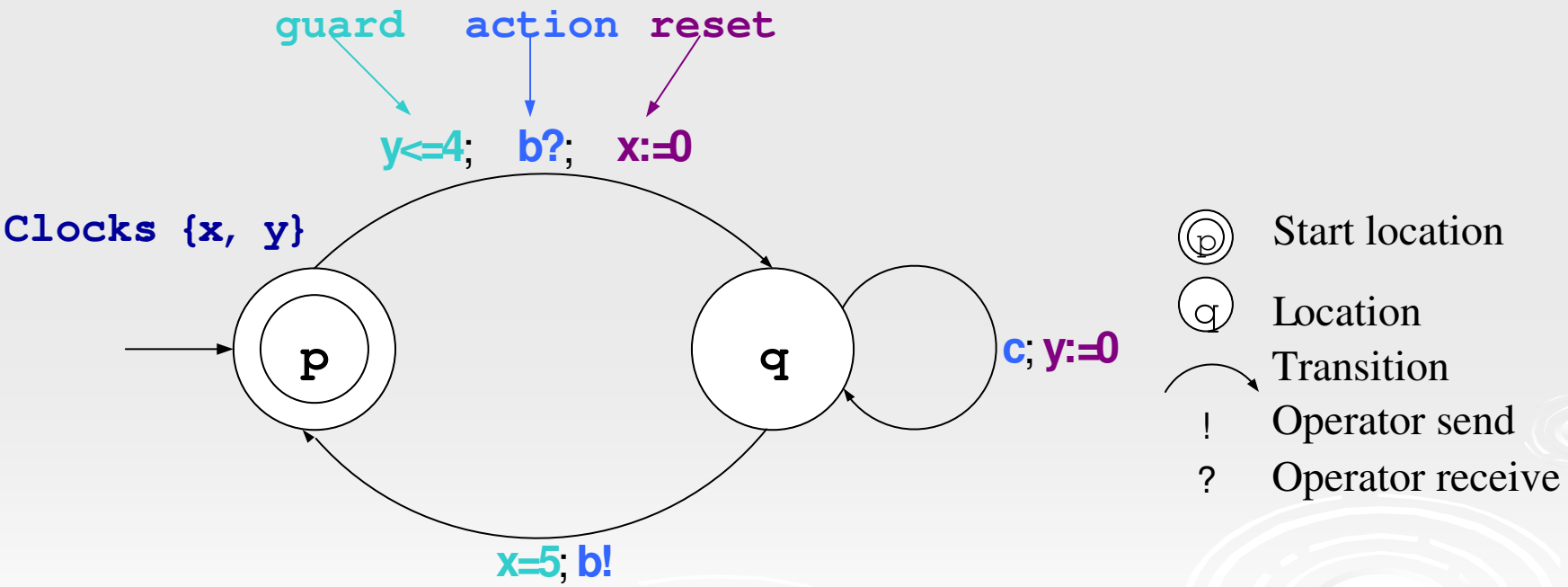
Timed Automata

- Classical finite state automata with clock variables and logical formulas on the clock (temporal constraints)



Outline

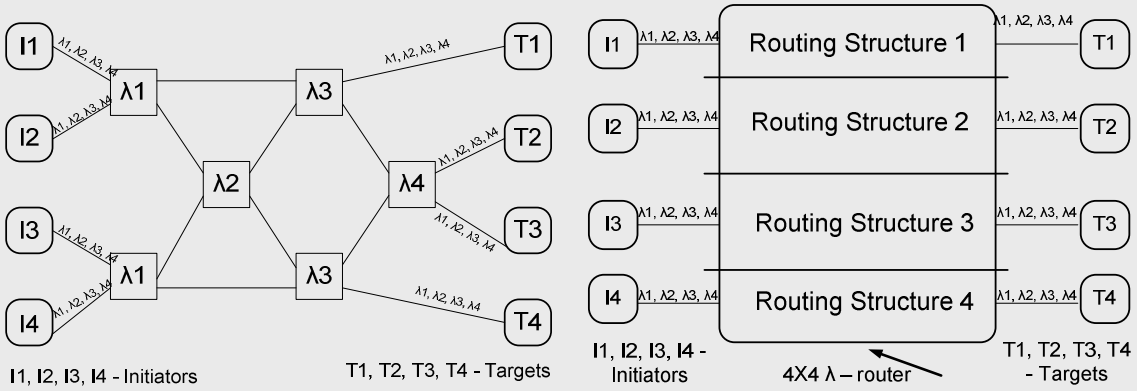
- Basic concepts
- **Optical NoCs modeling and simulation**
- Optical NoCs formal verification
- Conclusions

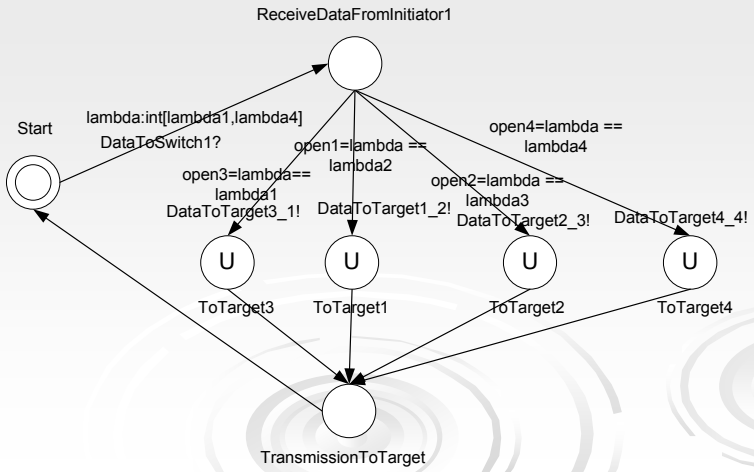
Optical NoC modeling and simulation

- *Challenge*: complex models (contention free)
  - Require a large number of timed automata
  - Verification is time consuming
- *Methodology*: two steps to deal with the state explosion
  - The first step - the modeling and the formal verification of the behavior of the network at a high level of abstraction.
  - The second step – the modeling and the formal verification of the behavior of the network at a lower level of abstraction, on segments of the network.

Optical NoC modeling and simulation

- First step – high level of abstraction





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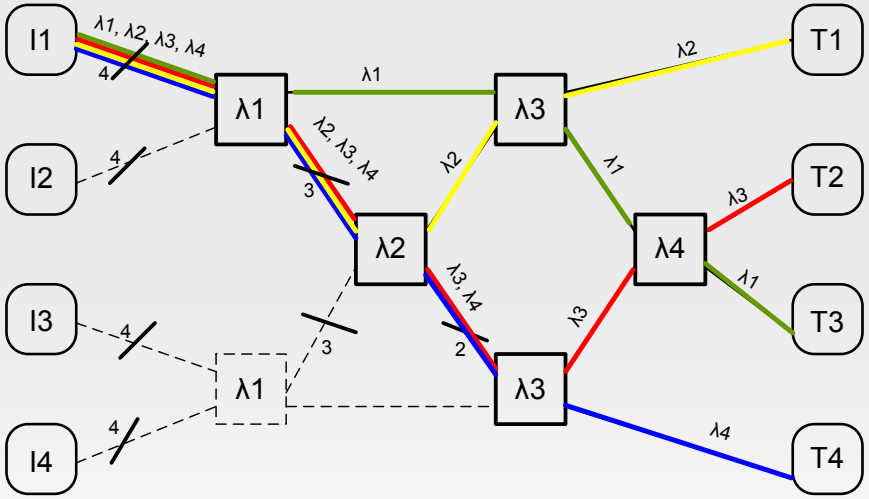
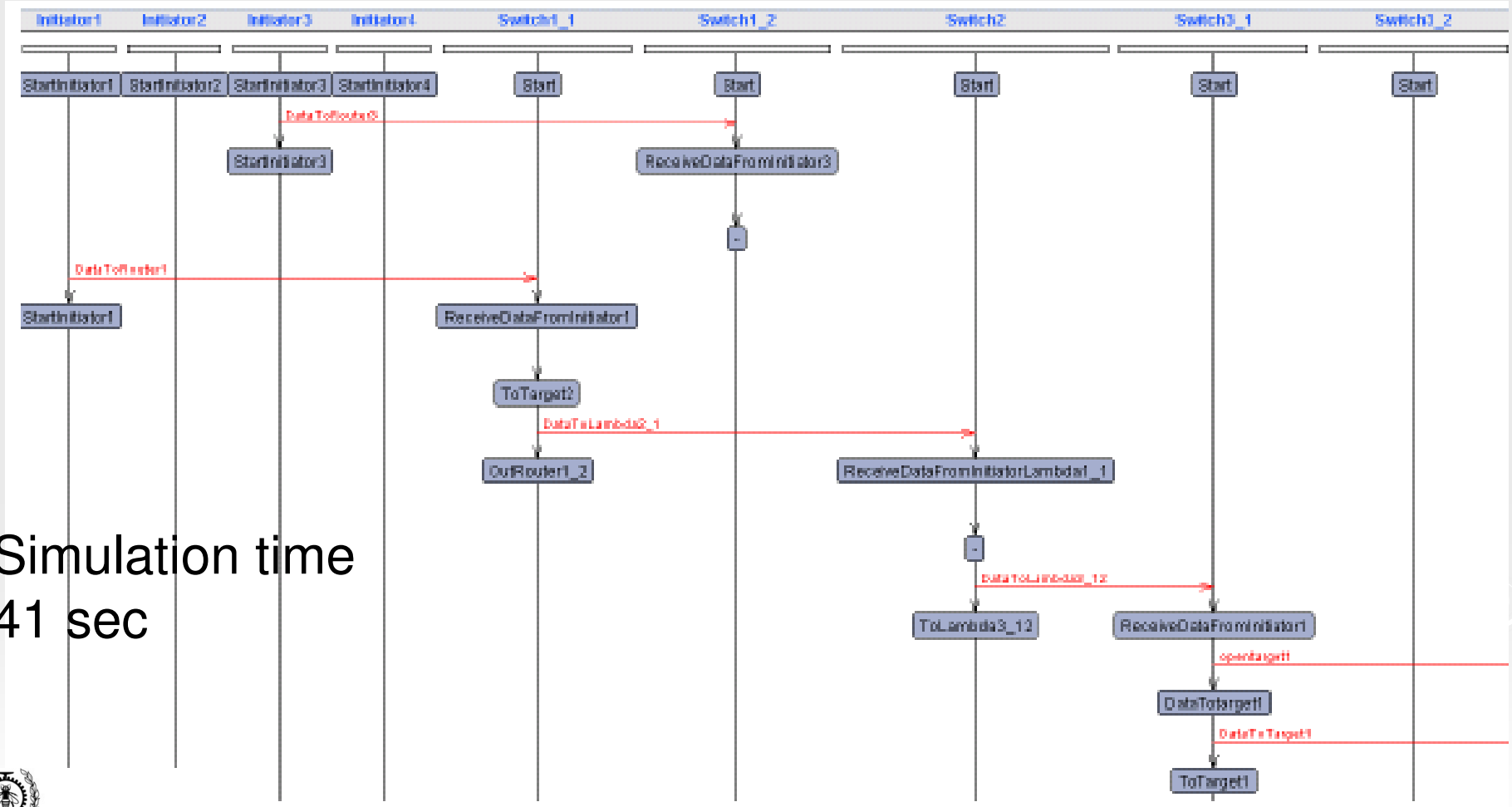
Optical NoC modeling and simulation

- Second step - lower level of abstraction and partition



Simulation capture



Simulation time
41 sec

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Verified properties

- No deadlock
- Simultaneous wavelength can be sent through different switches in the same time
- Routing correctness
- All locations in an automaton modeling a switch or processing elements are eventually taken

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Summary

- System-Level modeling of an Optical NoC
  - First results for global modeling of a passive optical network on chip behavior
  - Formal verification of a passive optical network on chip behavior
- Cooperation between Physical Designers and System-Level Designers
  - Physical Design Team
    - Ecole Centrale de Lyon (Prof. Ian O`Connor)
  - System-Level Design Team
    - Ecole Polytechnique de Montreal – global modeling and simulation for Opto-Electrical MPSoC
- Future work – the integration of the passive and the active optical devices and IC in order to realize the global execution model of the ONoC