Per Pesse Power Transducer Deployment Schedule Logical Platform Platform Mapping Physical Platfore Physical Platfore Physical Platfore Province of the power of the powe



Model-based specification, analysis and synthesis of servo controllers for lithoscanners

Ramon Schiffelers (ASML, TU/e), Wilbert Alberts (ASML), Jeroen Voeten (ESI, TU/e)

Embedded Systems



1. About ASML

ASML is the world's largest supplier of lithography systems for the semiconductor industry

ASML designs and develops machines that are used to print circuits on silicon wafers, to produce IC chips

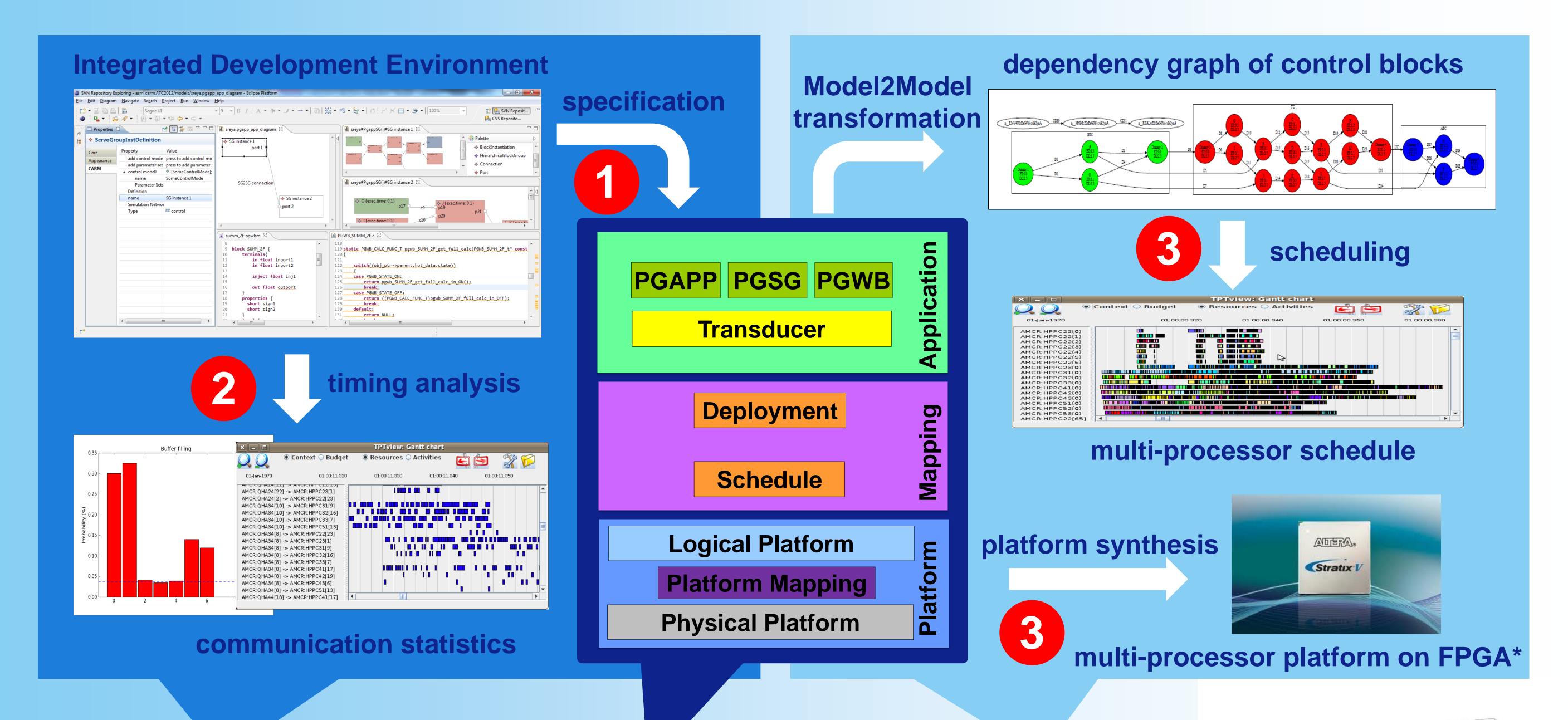
2. Servo Control

Scanners contain numerous servo control systems

One such systems positions a 15 kg wafer position table in six degrees of freedom with nanometer accuracy at acceleration speeds exceeding 110 G

4. CARM 2G

- Specification of controllers and platforms using Domain Specific Languages
- Analysis of sample frequencies, IO delays, processor and network loads
- Synthesis of software code, multi-processor platforms on FPGAs* and schedules



Specification & Analysis models @ design time

Domain Specific Languages for Formal Specification models @ pivot

Integration & Initialization models @ TWINSCAN



3. Challenges

Simultaneous productivity and accuracy improvement is a constant drive in the semiconductor industry

As a results the number of servo control systems, their dependencies, servo bandwidth and sampling rates all increase dramatically

Multi-disciplinary environment is indispensable to develop predictable controllers with a predictable lead time

5. Conclusions

CARM 2G successfully applied within ASML
Complexity reduction by concisely capturing the servo domain
Improved communication among developers
Design decisions taken on basis of analysis results
Efficiency increase through automated synthesis

DSLs should be enhanced with facilities for modular design

Syntactic facilities for concise specification should be separated from the underlying semantic models needed for analysis and synthesis

^{*} Executed in an ASML research environment only.